IDEC Chip Design Contest

A Four-Phase Digital Buck Converter With MDLL-Based Adaptive Switching Frequency Compensation

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1. Introduction

DC-DC buck converters are essential in the PMUs of SoCs, enabling efficient power delivery and voltage regulation from batteries to various subsystems within the chip. The power efficiency and transient response time of a buck converter are determined by its switching frequency. The trade-off where a higher frequency reduces efficiency, and a lower frequency slows the transient response time is a key design consideration for buck converters in modern SoCs. To address these limitations, we propose a 4-phase digital buck converter incorporating a multiplying delay-locked loop (MDLL) based adaptive switching frequency compensation (ASFC).

2. Description

Fig. 1. is overall block diagram, which consists of a digital PID-based voltage loop and an MDLL-based frequency loop. The equency loop performs two critical functions. 1) it dynamically controls the DPWM, maintaining a regulated FSW generated by the MDLL. 2) it generates a regulated VREF through MDLL, which is supplied to the CT-ADC. The MDLL is designed to adjust both FSW and VREF simultaneously and functions as an ASFC mechanism that immediately responds to load current variations. By adaptively tuning FSW, the converter ensures a fast response when ILOAD rises and minimizes losses when ILOAD falls. The adaptive control loop of the proposed 4-phase buck converter guarantees stable and efficient operation across diverse load conditions.

3. TOP Block

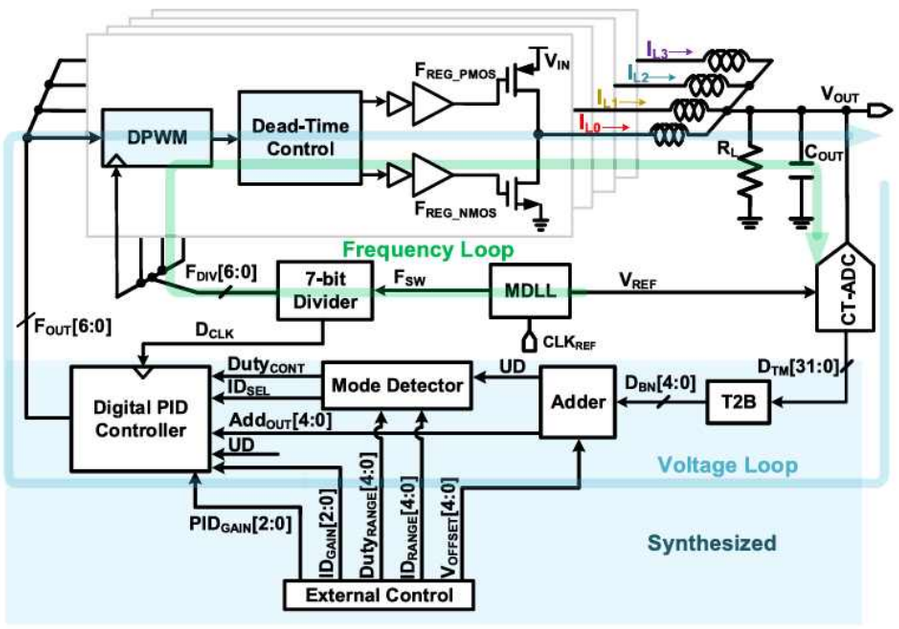

Fig 1. Overall block diagram of the proposed 4-phase digital buck converter

4. MDLL Block

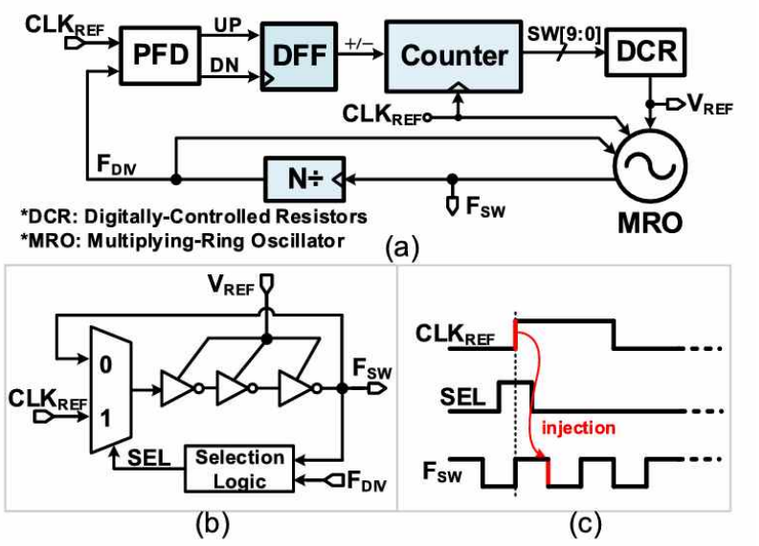

Fig 2. Detailed diagram of the MDLL (a) block diagram, (b) MRO, (c) MRO waveforms

5. Measurement

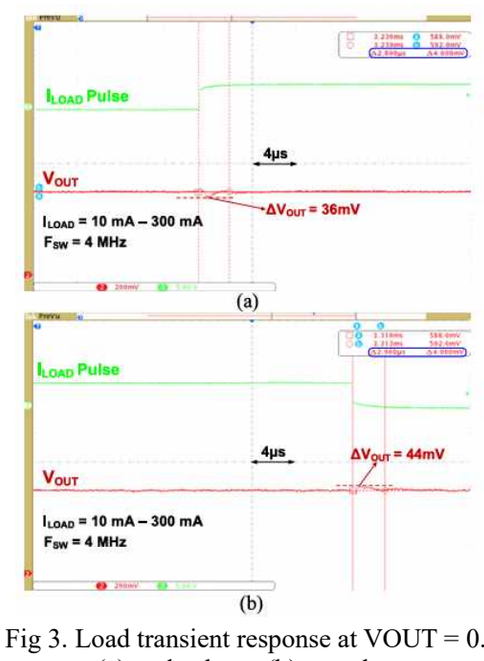

Fig 3. Load transient response at VOUT = 0.5V
(a) undershoot, (b) overshoot

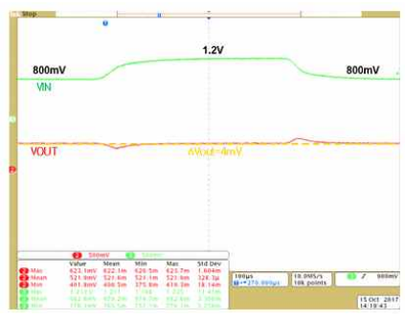

Fig 4. Line transient response at VOUT = 0.5V

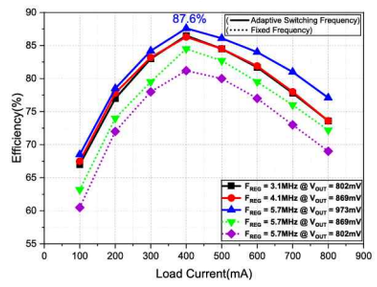

Fig 5. Power efficiency at various conditions

6. Chip Micrograph & PCB

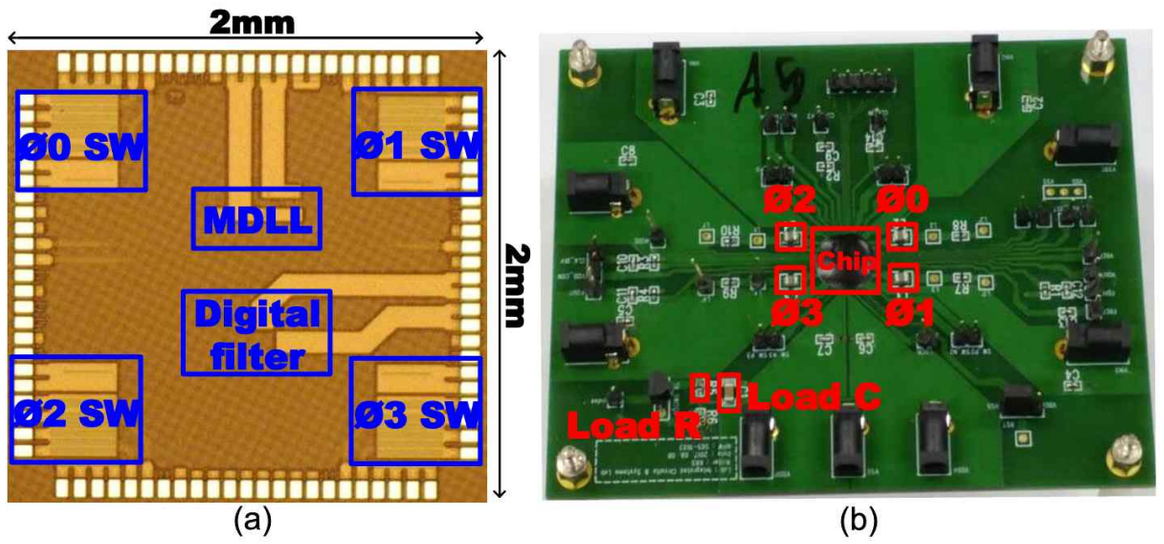

Fig 6. (a) Micro photograph of chip, (b) Prototype PCB

7. Conclusion

The proposed 4-phase digital buck converter, incorporating an MDLL-based ASFC technique, significantly enhances power efficiency and load regulation in digital PMU applications. The innovative use of the MDLL-based ASFC allows the converter to dynamically adjust its switching frequency in response to varying load conditions, thereby minimizing conduction and switching losses. This adaptive approach not only improves the converter's overall efficiency, achieving a peak efficiency of 87.6%, but also effectively reduces output voltage ripples, enhancing transient response time. Measurement results demonstrate that the proposed buck converter recovers from an undershoot of 36 mV within 2.8 μs for a load current step of 290 mA. This design was fabricated in a 65-nm CMOS process, occupying an overall chip area of 2 mm^2. The successful implementation and measurement results demonstrate that this design is highly suitable for modern SoC applications .

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